

Figure 6 schematically shows an alternative for the test unit for five inputs and two outputs. This figure corresponds with the Example 3 above. The test unit 406 has a three-input XOR gate 602 which implements the required exclusive-or function between o1 and i1, i2 and i3. The test unit further has a three-input XOR gate 604 which implements the
5 exclusive-or function between the input pins i3, i4 and i5 and the output pin o2.

The following table gives the patterns for Example 3 together with the required outputs.

pattern	iiii	oo
number	12345	12
1	00000	00
2	10000	10
3	01000	10
4	00100	11
5	00010	01
6	00001	01
7	11111	11
8	01111	01
9	10111	01
10	11011	00
11	11101	10
12	11110	10

10 It is to be noted that the above-mentioned embodiments illustrate rather than limit the invention and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim.